

**STATIC RANDOM ACCESS MEMORY DEVICE HAVING  
REDUCED LEAKAGE CURRENT DURING ACTIVE  
MODE AND A METHOD OF OPERATING THEREOF**

**ABSTRACT OF THE DISCLOSURE**

An Static Random Access Memory (SRAM) device and a method of operating the same. In one embodiment, the SRAM device includes:

- (1) an SRAM array coupled to row peripheral circuitry by a word line and coupled to column peripheral circuitry by bit lines and
- (2) an array low voltage control circuitry that provides an enhanced low operating voltage  $V_{ESS}$  to the SRAM array during at least a portion of an active mode thereof.